

## Hit List

Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs
Generate OACS				

### Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: US 5975097 A

L15: Entry 1 of 2

File: USPT

Nov 2, 1999

US-PAT-NO: 5975097

DOCUMENT-IDENTIFIER: US 5975097 A

TITLE: Processing apparatus for target processing substrate

DATE-ISSUED: November 2, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yonemizu; Akira	Kumamoto			JP
Kudou; Hiroyuki	Nishikoshimachi			JP
Akimoto; Masami	Kumamoto			JP

US-CL-CURRENT: 134/95.2; 134/147, 134/153, 134/902

ABSTRACT:

A processing apparatus of this invention has an openable window portion for transferring a target processing substrate, and an inlet port for introducing the outer atmosphere. Further, the processing apparatus includes a closed processing chamber for performing predetermined processing for the target processing substrate transferred via the window portion, an exhaust means for evacuating the interior of the processing chamber, and an opening/closing mechanism for closing the inlet port, and opening the inlet port when the pressure in the processing chamber is negative.

18 Claims, 21 Drawing figures

Exemplary Claim Number: 13

Number of Drawing Sheets: 14

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw De
------	-------	----------	-------	--------	----------------	------	-----------	--	--	--------	------	---------

☐ 2. Document ID: US 5258093 A

L15: Entry 2 of 2

File: USPT

Nov 2, 1993

US-PAT-NO: 5258093

DOCUMENT-IDENTIFIER: US 5258093 A

h e b b g e e e f e g e f b e

TITLE: Procss for fabricating a ferroelectric capacitor in a semiconductor device

DATE-ISSUED: November 2, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Maniar; Papu D.	Austin	TX		

US-CL-CURRENT: 438/3; 134/3, 134/41, 216/101, 252/79.2, 252/79.3, 257/E21.009,  
257/E21.228, 257/E21.251, 257/E21.309, 438/16, 438/396

ABSTRACT:

An etching process for the patterning of electrodes and a ferroelectric dielectric layer in a ferroelectric capacitor, which is formed in a semiconductor device, is disclosed. A series of overlying layers including a first electrode layer (16), a ferroelectric layer (18), and a second electrode layer (20) are etched to form a ferroelectric capacitor (14) on a semiconductor substrate (10). The second electrode layer (20) is selectively etched in a first aqueous solution containing hydrochloric acid, nitric acid, and a metal etching compound comprised of phosphoric acid, nitric acid, and acetic acid. The ferroelectric layer (18) is selectively etched in a second aqueous solution containing hydrogen peroxide, hydrofluoric acid, and nitric acid. The etch rate of the ferroelectric layer in the second aqueous solution is controlled by selection of the relative concentration of the chemicals used to form the solution. The wet chemical etching process of the invention can be combined with a dry etching process for the purpose of removing dry etch residue following formation of the ferroelectric capacitor (14).

13 Claims, 3 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 2

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	RMAC	Draw. De
------	-------	----------	-------	--------	----------------	------	-----------	--	--	--------	------	----------

Clear	Generate Collection	Print	Fwd Refs	Backwd Refs	Generate OACS
-------	---------------------	-------	----------	-------------	---------------

Term	Documents
"5258093"	1
5258093S	0
"5975097"	1
5975097S	0
("5258093" OR "5975097").PN..USPT.	2
((("5258093) OR (5975097)).PN.).USPT.	2

Display Format:

[Previous Page](#)

[Next Page](#)

[Go to Doc#](#)

h e b b g e e e f e g e f b e